TWIN-RELECT

SUMMER WORKSHOPS 2026

TWINRELECT

TWINNING FOR EXCELLENCE IN RELIABLE ELECTRONICS

# 2nd Scientific Workshop on Fault-Tolerant Design and Real-Time Reliability Monitoring

## 4th Research Management & Administration Workshop

**13-15** & **16-17** **July 2026**

**Event Hall**
Sekeri – Cheiden Str
ECE Building
Volos – Greece

EVENT PROGRAM

Grant Agreement № 101160314

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UK Research and Innovation

**The goal of TWIN-RELECT project is to boost the scientific and innovation capacity of University of Thessaly in the design of reliable electronic systems through strategic networking with three advanced partners: IHP - Institute for High Performance Microelectronics from Germany, National Center for Scientific Research (CNRS) from France, and University of Manchester from United Kingdom.**

*Under the Grant Agreement Nº 101160314. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. The European Union can not be held responsible for them.*

# PARTNERS

The University of Thessaly (UTH), founded in 1984, has expanded across several cities in Greece, offering 8 Schools, 35 Departments, and 90+ postgraduate master's programs. The CAS Lab team, part of the ECE Department, specializing in Electronic Design Automation (EDA) research will participate in the project.

The Leibniz Institute for High-Performance Microelectronics (IHP) specializes in fault-tolerant circuit design for safety-critical applications. The institute, based in Frankfurt (Oder), Germany, has advanced tools for circuit testing and is involved in the EU-funded MORAL project, developing rad-hard microcontrollers for space applications.

The National Center for Scientific Research (CNRS) is represented in the project by the IES (Institute of Electronics and Systems), a joint research unit with the University of Montpellier. The IES RADIAC team, specializing in electronics reliability in radiation environments, plays a key role in international projects and is involved in developing radiation sensors, simulation tools, and failure analysis methods.

The University of Montpellier, established in 1220, is one of the oldest universities in the world. It was reunified in 2015 and ranks among the top 200 universities globally, securing 55th place in the Reuters Most Innovative Universities 2018 and 98th in the University Ranking by Academic Performance 2021–2022.

The University of Manchester's Advanced Processor Technologies (APT) group, led by Prof. Steve Furber, focuses on brain-inspired computing and neuromorphic systems for edge AI applications. They are developing low-power, fault-tolerant solutions, including hybrid SNN-ANN systems, and addressing the lack of electronic design automation tools for reliable, cost-effective neuromorphic architectures.

# SCIENTIFIC PROGRAM

## Monday, 13 July 2026

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| 09:00 - 09:30 | **Registration** |
| 09:30 - 09:45 | **Introduction**<br>Prof. Christos Sotiriou, University of Thessaly |
| 09:45 - 10:30 | **Reliability vs. Security: Friends or Foes?**<br>Dr. Mahdi Taheri, Brandenburg University of Technology (BTU) Cottbus-Senftenberg |
| 10:30 - 11:00 | **Coffee Break** |
| 11:00 - 12:00 | **Radiation Hardness Assurance at ESA – from low to high risk missions**<br>Dr. Viyas Gupta, European Space Agency (ESA) |
| 12:00 - 12:45 | **Customized Algorithm-Based Fault Tolerance for Modern AI Accelerators**<br>Prof. Giorgos Dimitrakopoulos, Democritus University of Thrace |
| 12:45 - 13:45 | **Lunch Break** |
| 13:45 - 15:00 | **PhD Forum** |
| 15:00 - 16:00 | **IHP - UTH Chip Fabrication Meeting**<br>Closed Meeting |

# SCIENTIFIC PROGRAM

## Monday, 13 July 2026

## Phd Forum

**Cross-Layer Reliability Analysis of Slimmable Neural Networks under Permanent Faults**
Nikolaos Zazatis, University of Thessaly

**Soft Error Reliability Analysis & Hardening of NVDLA MAC Units**
Nikolaos Chatzivangelis, University of Thessaly

**3MLR: An Investigation of Moment-Matched Mutual Ladder-based Reduction for VLSI Static Timing Analysis**
Aikaterini Tsilingiri, University of Thessaly

**Efficient Capacitance Extraction for Accurate STA-based reliability Analysis**
Kainat Naeem, University of Thessaly

**Post placement timing optimisation on synchronous and asynchronous designs under power constraints**
Dimitris Tsalapatas, University of Thessaly

**Energy efficient FPGA Spiking Neural Networks**
Dimitrios Sekertzis, Democritus University of Thrace

**Acceleration of FHE/PCQ workloads on AI ASICs**
George Alexakis, Democritus University of Thrace

**Adaptive Region-Aware Reinforcement Learning for Multi-Objective VLSI Placement Refinement**
Foteini Oikonomou, University of Thessaly

**Low-cost AI-based Error Prediction**
Nikolaos Kostakis, University of Thessaly

## Tuesday, 14 July 2026

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| 09:00 - 09:45 | **Radiation Effects to FPGAs: An Overview**<br>Dr. George Tsiligiannis, Silicon Highway Technologies (SiHi) |
| 09:45 - 10:30 | **Current experiences and capabilities of open source EDA tools for mixed signal chip designs**<br>Dr. Juan Sebastian Moya-Baquero, International Iberian Nanotechnology Laboratory (INL) & SymbioticEDA |
| 10:30 - 11:00 | **Coffee Break** |
| 11:00 - 11:45 | **CERN Radiation Hardness Assurance (RHA) for Accelerator Electronics**<br>Dr. Salvatore Danzeca, CERN |
| 11:45 - 12:30 | **Reliability Challenges in Computing-in-Memory Systems**<br>Prof. Yiorgos Tsiatouhas, Department of Computer Science and Engineering, University of Ioannina |
| 12:30 - 13:15 | **Lunch Break** |
| 13:15 - 13:45 | **An Overview of On-Chip Particle Detectors for Self-Adaptive Integrated Circuits for Space**<br>Dr. Marko Andjelkovic, IHP - Leibniz Institute for High Performance Microelectronics |
| 13:45 - 14:15 | **Cross-Layer Analysis of Permanent Faults in Asynchronous NoCs for Neuromorphic Computing**<br>Prof. Davide Bertozzi, University of Manchester |
| 14:15 - 14:45 | **Error Monitoring and Hardening on the HARV (RISC-V) Microcontroller**<br>Prof. Luigi Dilillo, University of Montpellier |
| 14:45 - 15:00 | **Coffee Break** |
| 15:00 - 16:00 | **Closing the gap between Reliability Physics, EDA and Circuit Design**<br>Mr. George Konstadinidis, Technology and HPC/AI HW Design consultant |

## Wednesday, 15 July 2026

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| 09:00 - 09:45 | **Radiation-Hard Power Management and Control Circuits for the ATLAS Pixel Detector High-Luminosity Upgrade**<br>Prof. Michael Athanassios Karagounis, Dortmund University of Applied Sciences and Arts |
| 09:45 - 10:30 | **Neural Network Quantization**<br>Prof. Milan Dinčić, Faculty of Electronic Engineering, University of Niš |
| 10:30 - 11:00 | **Coffee Break** |
| 11:00 - 11:45 | **Open and Intelligent High-Level Synthesis Flows for Secure, Reliable, and Efficient Chip Design**<br>Prof. Christian Pilato, Politecnico di Milano |
| 11:45 - 12:30 | **Beyond Worst-Case Design for Energy-Conscious Dependable Architectures**<br>Prof. Georgios Karakonstantis, University of Thessaly |
| 12:30 - 13:30 | **Lunch Break** |
| 13:30 - 14:00 | **Combined Effects of Ionizing and Non-Ionizing Radiation: From Simulation to Practical Experiments**<br>Dr. Fabian Luis Vargas – IHP - Leibniz Institute for High Performance Microelectronics |
| 14:00 - 14:30 | **DFT Reuse Across Silicon Lifetime**<br>Dr. Artur Jutman, TalTech - Tallinn University of Technology and Testonica Lab |
| 14:30 - 15:00 | **STA-Based Radiation Hardening Framework**<br>Nikolaos Chatzivangelis, University of Thessaly<br>Nikolaos Zazatis, University of Thessaly |
| 15:00 - 16:00 | **TWIN-RELECT Consortium Meeting**<br>Closed Meeting |
| 20:00 - 23:00 | **Social Event** |

# RESEARCH MANAGEMENT

## Thursday, 16 July 2026

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| 09:00 - 09:45 | **Welcome Session & Overview of Research Management Progress**<br>Prof. Christos Sotiriou, University of Thessaly |
| 09:45 - 10:30 | **Scientific Management: Balancing Innovation and Critical Services**<br>Dr. Salvatore Danzeca, CERN |
| 10:30 - 11:00 | **Coffee Break** |
| 11:00 - 11:45 | **From Proposal to Ecosystem: Building Successful European Research and Innovation Projects**<br>Prof. Christian Pilato, Politecnico di Milano |
| 11:45 - 12:30 | **How to do R&D with ESA's TEC Directorate**<br>Dr. Viyas Gupta, European Space Agency (ESA) |
| 12:30 - 13:30 | **Lunch Break** |
| 13:30 - 14:15 | **Innovation Management in the Age of LLMs: Accelerating Complex System Design**<br>Prof. John Goodacre, Department of Computer Science, University of Manchester |
| 14:15 - 14:45 | **Open source chip design tools: What for? In the past, the present and the future**<br>Mr. Edmund Humenberger, SymbioticEDA |
| 14:45 - 15:45 | **Managing Large Multi-Country Consortia**<br>Open Discussion |

## Friday, 17 July 2026

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| 09:00 - 09:45 | **Proposal Preparation: Lessons Learned from the AIDA4Edge and PEMS-ML Projects**<br>Prof. Milan Dinčić, Faculty of Electronic Engineering, University of Niš |
| 09:45 - 10:30 | **The path from an R&D idea to a product**<br>Mr. George Konstadinidis, Technology and HPC/AI HW Design consultant |
| 10:30 - 11:00 | **Coffee Break** |
| 11:00 - 11:45 | **European Project Design and Management: Challenges and Opportunities**<br>Mr. Charalampos Samantzis, Center of International Education University of Thessaly |
| 11:45 - 12:30 | **EU-Band: A D-Band Joint Communication and Sensing System in a Eurostars Project**<br>Dr. Karthik Krishnegowda, IHP - Leibniz Institute for High Performance Microelectronics |
| 12:30 - 13:30 | **Lunch Break** |
| 13:30 - 13:50 | **Meet the IEEE Student Branch & WIE Affinity Group of Volos**<br>Panagiotis Balamotis, University of Thessaly<br>Eleftheria Litou, University of Thessaly<br>Evangelos Toris, University of Thessaly |
| 13:50 - 14:00 | **Closing Session**<br>Prof. Christos Sotiriou, University of Thessaly |

**Workshops Coordinator:** Dr. Nikolaos Sketopoulos, University of Thessaly

# KEYNOTE SPEAKERS

## Dr. Viyas Gupta: Radiation Hardness Assurance at ESA – from low to high risk missions

**Abstract:** This talk will briefly introduce what RHA (Radiation Hardness Assurance) is and how it is tackled in ESA space projects. In particular, the talk will focus on how RHA is performed on common ESA low-risk missions but also how the RHA process is tailored to higher-risk ESA missions such as small satellites and CubeSat missions.

## Dr. Viyas Gupta: How to do R&D with ESA's TEC Directorate

**Abstract:** This talk will briefly list & explain the different R&D programmes of the TEC Directorate in ESA.

**Bio:** Viyas Gupta graduated with a PhD in radiation effects on space electronics from the University of Montpellier. He worked as a systems engineer on CubeSat related projects as a young graduate trainee (YGT) in the ESA Education Office, as well as during his PhD. He also worked as an education engineer in ESEC on the development of new training sessions in different space fields for the Training & Learning Programme as well as providing engineering support to the ESA Fly Your Satellite programme. Currently he is working as a Radiation Effects Engineer at ESTEC in the Netherlands, providing RHA support to various ESA space missions including deep space CubeSat missions.

## Dr. George Tsiligiannis: Radiation Effects to FPGAs: An Overview

**Abstract:** FPGAs have served as the fundamental building block of applications operating in challenging environments. Their use and complexity has grown exponentially in the last decade, making their qualification and mitigation a rather challenging task. In this presentation Dr Georgios Tsiligiannis will be talking about how particles interact with FPGAs and their internal resources such as DSPs, BRAMs, Hardcoded MCUs, and the challenges of testing.

**Bio:** Dr Georgios Tsiligiannis is currently a Principal Design Engineer at Silicon-Highway Technologies. He has a background on ASIC Design, FPGA Design, and Radiation Hardness Assurance. He has held positions at the University of Montpellier, CERN, JPL, Applied Materials and Qualcomm. He has performed research on Radiation Effects to Memories, FPGAs and MCUs among others. His current role is to help bridge the gap between EDA tools and Radiation Hardness, leveraging STA-based solutions.

# Prof. Giorgos Dimitrakopoulos: Customized Algorithm-Based Fault Tolerance for Modern AI Accelerators

**Abstract:** Hardware accelerators powering modern machine learning workloads, such as Convolutional Neural Networks (CNNs), Graph Convolutional Networks (GCNs), and LLM-based Transformers, require robust protection against random hardware faults. While Algorithm-Based Fault Tolerance (ABFT) is a proven method for online error detection, applying generic ABFT techniques to ML kernels introduces redundant checks and excessive computational overhead. This presentation highlights the need to customize fault-tolerance structures to the mathematical properties of each ML algorithm. By leveraging workload-aware transformations rather than off-the-shelf solutions, we derive highly efficient custom checkers that detect errors rapidly and at a fraction of the traditional cost. We demonstrate this unified design philosophy through three recent architectural breakthroughs. In CNNs, exploiting the mathematical invariance of convolutions allows us to predict output checksums using only border pixels, drastically reducing power and memory requirements. In GCNs, we eliminate the overhead of validating multiple matrix multiplications per layer by collapsing the verification into a single three-matrix-product checksum. Finally, for attention mechanisms in LLMs, we show that a unified online checksum spanning the entire query-key-value pipeline can overcome the non-linear barrier introduced by intermediate softmax normalization. Together, these examples illustrate that maximizing fault-tolerance efficiency in modern AI accelerators requires hardware checkers to be deeply co-designed with the unique algorithmic behaviors they protect.

**Bio:** Giorgos Dimitrakopoulos is a Professor of Digital Integrated Circuits in the Department of Electrical and Computer Engineering at the Democritus University of Thrace in Xanthi, Greece. He received his B.S., M.Sc., and Ph.D. degrees in Computer Engineering from the University of Patras, Greece, in 2001, 2003, and 2007, respectively. His research spans Digital VLSI design, computer architecture, and EDA physical synthesis. Currently, his research group focuses on agile chip design, utilizing both RTL and high-level synthesis (HLS) design flows, to develop energy-efficient data-parallel accelerators for machine learning workloads, RISC-V processors, and privacy-preserving technologies. Also, he is also actively engaged in digital IC verification and low-cost functional safety. His research efforts have been funded by major industry partners, including Siemens EDA, Nokia Bell Labs, Infineon, Codasip, and SmartSilicon. Prof. Dimitrakopoulos received the HIPEAC Technology Transfer Award in 2015 and has co-authored two Best Paper Awards at the Design Automation and Test in Europe (DATE) Conference (2015, 2019). His Ph.D. students have been recognized within the VLSI and EDA communities, earning the EDAA Outstanding Dissertation Award in 2018, as well as Best Student Paper Awards at AICAS (2024) and MOCAST (2021).

## Prof. Christian Pilato: Open and Intelligent High-Level Synthesis Flows for Secure, Reliable, and Efficient Chip Design

**Abstract:** High-Level Synthesis (HLS) is becoming a key technology for improving productivity in modern chip design, especially for AI accelerators, heterogeneous architectures, and hardware/software co-design. This talk presents recent advances in open and AI-assisted design flows based on HLS methodologies. Topics include automated design-space exploration, AI-assisted RTL generation, integration with open-source EDA tools, and timing- and power-aware optimization
techniques. The presentation will also discuss how these methodologies can support more efficient, flexible, and reliable chip development while addressing verification, security, and long-term maintainability challenges in complex electronic systems.

## Prof. Christian Pilato: From Proposal to Ecosystem: Building Successful European Research and Innovation Projects

**Abstract:** European research projects are expected not only to produce scientific and technological results, but also to create industrial impact, support innovation ecosystems, and generate long-term value. This talk presents practical experiences and lessons learned from the preparation, coordination, and management of large-scale EU-funded projects in semiconductors and digital technologies. The presentation will cover the full lifecycle of collaborative projects, from identifying strategic opportunities and building international consortia to defining dissemination, exploitation, and technology transfer strategies. Particular attention will be devoted to ecosystem-building activities such as open innovation, training, standardization, stakeholder engagement, and collaboration between academia, industry, SMEs, and research centers. The talk will also discuss the challenges of balancing ambitious research goals with effective project management, financial and administrative requirements, and long-term sustainability beyond the end of the funded project.

**Bio:** Christian Pilato is an Associate Professor at Politecnico di Milano. He was a Postdoctoral Researcher at Columbia University and the University of Lugano and a Visiting Researcher at New York University, TU Delft, and Chalmers University of Technology. He received his Ph.D. in Information Technology from Politecnico di Milano in 2011. His research focuses on heterogeneous architectures, with particular emphasis on high-level synthesis, memory systems, hardware security, and open-source Electronic Design Automation (EDA) methodologies. He is currently the Coordinator of the ODE4EC-DIG project, funded by Chips JU, focused on open-source EDA flows for digital chip design. He was also the Scientific Coordinator of the H2020 EVEREST project. He served as Program Chair for EUC 2014, ICCD 2022, SAMOS XXIII, ICCD 2023, and SAMOS XXIV, and as General Chair of ICCD 2024. He is an Associate Editor for IEEE TCAD. He is a Senior Member of IEEE and ACM, a Member of HiPEAC and DISCOVER-US, and currently serves as Chair of the ACM SIGDA Executive Committee.

# Dr. Salvatore Danzeca: CERN Radiation Hardness Assurance (RHA) for Accelerator Electronics

**Abstract:** Radiation Hardness Assurance (RHA) at CERN is a structured qualification framework specifically developed to enable the reliable use of commercial off-the-shelf (COTS) electronic components in the radiation environments of particle accelerators. Given the large scale and distributed nature of CERN systems, the use of radiation-hardened components is often impractical due to cost, performance, and availability constraints. RHA therefore provides a risk-based methodology to qualify COTS devices for use in critical accelerator applications.

CERN accelerator environments are characterized by complex mixed radiation fields with particles of energies spanning from thermal up to several GeV. These environments differ significantly from space or nuclear reactor conditions and vary strongly with location and shielding, requiring application-specific qualification strategies. RHA addresses this by combining procurement, radiation lot quality acceptance test and representative irradiation testing.

The qualification process considers all relevant radiation effects, Total Ionizing Dose (TID), Displacement Damage (DD), and Single Event Effects (SEE). COTS components are subjected to exploratory radiation testing to identify sensitivities, followed by targeted qualification campaigns performed under representative biasing and operating conditions for the production lots. For destructive SEE such as latch-up or burnout, qualification requirements are derived from system-level constraints including radiation levels, number of deployed units, redundancy schemes, and acceptable annual failure rates. These requirements are then propagated to board- and component-level target cross-sections.

To control manufacturing variability inherent to COTS technologies, CERN applies strict traceability and lot-based qualification, including single-date-code procurement and radiation lot acceptance testing for production batches used in critical systems. Large-volume mixed-field irradiation facilities are essential to test hundreds or thousands of devices in a single campaign, enabling statistically meaningful upper limits on very low failure probabilities.

Through continuous refinement of testing methodologies, qualification criteria, and system-level risk analysis, CERN's RHA framework enables the effective and reliable deployment of COTS electronics in accelerator radiation environments, supporting long-term machine availability and operational safety.

# Dr. Salvatore Danzeca: Scientific Management: Balancing Innovation and Critical Services

**Abstract:** Scientific organization such as CERN must constantly balance cutting-edge research with the reliable operation of services that thousands of users depend on. This talk explores how these two goals can strengthen each other through effective management and engineering practices. Drawing on the experience of leading multidisciplinary engineering teams at the interface between research, electronics production, and radiation test services, this presentation explores practical approaches to balancing innovation with operational excellence. It highlights how organizational structures, shared engineering workflows, portfolio management, and data-driven decision making can create an environment where research and reliable service delivery reinforce one another. Through examples from CERN's Electronics Production and Radiation Test Services, the presentation discusses how common tools, regular cross-functional interactions, and carefully designed project portfolios help bridge different engineering cultures and transform collaboration into a measurable outcome. Particular attention is given to the role of performance indicators, strategic portfolio steering, and knowledge preservation in supporting informed decisions within a highly complex technical environment.

**Bio:** Dr. Salvatore Danzeca is the Section Leader of the Electronics Production and Radiation Tolerance (EPR) team in the Beams Department at CERN, where he leads CERN-wide activities on radiation-tolerant electronics, radiation testing and radiation monitoring for accelerator systems. His mandate includes providing radiation testing and qualification services for electronic components and systems used across the CERN accelerator complex, ensuring their reliable operation in harsh radiation environments. He is responsible for the operation, monitoring and maintenance of more than 500 radiation monitoring devices installed in the Large Hadron Collider (LHC) and in its injector chain, supporting dosimetry, machine protection and long-term reliability studies. Dr. Danzeca also oversees two of CERN’s key radiation test facilities, CHARM (CERN High-energy AcceleRator Mixed-field facility) and CC60 (a cobalt-60 irradiation facility), which are used to qualify electronics for accelerator. As an academic researcher, he has co-authored numerous publications on radiation effects, dosimetry and the radiation environment of the LHC, contributing to the development of robust electronics and monitoring strategies for high-energy physics experiments. He regularly collaborates with international partners and contributes to working groups and workshops on radiation to electronics (R2E) and radiation hardness assurance, bridging accelerator needs with industrial and space communities.

# Dr. Juan Sebastian Moya-Baquero: Current experiences and capabilities of open source EDA tools for mixed signal chip designs

**Abstract:** Open-source process design kits (PDKs) and electronic design automation tools are creating new opportunities for hands-on training, prototyping and collaborative development in integrated circuit design. This presentation provides a practical demonstration of mixed-signal design and simulation using open-source PDKs. It covers schematic-level simulation, layout implementation, parasitic extraction and post-layout verification. The presentation also discusses how self-checking tests can be applied to analog circuit design to facilitate integration into continuous integration and continuous deployment workflows. Automating simulation execution, metric extraction, pass/fail evaluation and report generation allows for more systematic verification of analog and mixed-signal blocks and their integration into reproducible chip design flows. This methodology is presented within the context of BlueGarden, SymbioticEDA's managed open-source IC design environment. BlueGarden combines reproducible Docker-based toolchains, open-source EDA tools, PDK support and CI/CD infrastructure for chip development. BlueGarden is presented as a managed platform unifying design activity, repositories, automation, verification and team-based access to open-source chip design environments. The presentation also reports on recent SymbioticEDA training and outreach activities using BlueGarden, including practical microelectronics training at the University of Aveiro, training activities funded by the IEEE in Colombia, and collaboration with the Hellenic Chips Competence Centre to support university-led training programmes in open-source and custom EDA tool flows. The talk highlights the importance of structured training, reproducible environments, automated verification, and fabrication, based on the experiences acquired in integrated circuit design training and real tape-out activities through ChipsEU- and IEEE-related initiatives.

**Bio:** Juan Sebastian Moya-Baquero is an electrical and electronics engineer specializing in analog, mixed-signal, and RF integrated circuit design, with experience in commercial CMOS technologies and open-source PDKs such as sky130A, gf180mcuD, and ihp-sg13g2. He is currently a Postdoctoral Researcher in IC Design and Design Flow at the International Iberian Nanotechnology Laboratory, where he works on CMOS circuit design, PDK development, design-flow automation, and EDA tool integration. He also works as a Mixed-Signal Designer at Symbiotic EDA, contributing to IHP 130 nm BiCMOS mixed-signal flows, tool validation, CI/CD support, and documentation. His academic background includes a Ph.D. in Electronics Engineering, a Master's degree in Integrated Circuits, and a Bachelor's degree in Electronics and Electrical Engineering. He has teaching and project experience in analog and digital IC design, including oscillators, LDOs, brown-out detectors, RFID systems, NFC circuits, high-speed interface blocks, and CMOS analog cells. He is also actively involved in IEEE initiatives focused on semiconductor education, open-source IC design, and workforce development.

# Edmund Humenberger: Open source chip design tools: What for? In the past, the present and the future

**Abstract:** Open-source chip design has moved from a fragmented set of academic and community tools toward a more practical ecosystem for education, prototyping, and early-stage semiconductor development. For decades, integrated circuit design depended mainly on proprietary Electronic Design Automation tools, confidential Process Design Kits, and fabrication access controlled through industrial or institutional partnerships. This created high barriers for universities, small research groups, startups, and emerging semiconductor communities. The recent release of open Process Design Kits such as SkyWater Sky130A, GlobalFoundries gf180mcuD, and IHP-SG13G2 has changed this landscape by enabling public access to manufacturable semiconductor technologies. In parallel, initiatives such as Efabless, ChipFoundry, Tiny Tapeout, IEEE PICO, UNIC-CASS, ChipPractice, and the IEEE Open Silicon Initiative have connected open design infrastructure with training, mentoring, community participation, and tape-out opportunities. However, open PDKs and individual tools alone are not sufficient. Practical chip design requires reproducible toolchains, maintained environments, workflow integration, verification infrastructure, and user support. This presentation traces the past, present, and future of open-source chip design tools, from early community-driven EDA development to today's managed open-source design environments. It discusses how platforms such as BlueGarden aim to transform open tools into reliable, Docker-based and CI/CD-enabled engineering environments for education, research, and professional design work. The presentation argues that the future of open-source chip design will depend not only on more open technologies, but also on sustainable infrastructure, institutional support, fabrication pathways, and educational models that allow students and engineers to move from theory to real manufactured chips.

**Bio:** Edmund Humenberger is CEO of Symbiotic EDA, a Vienna-based company developing and supporting open-source EDA workflows for FPGA and chip design. His work focuses on making hardware development more accessible through open FPGA tools, reproducible chip-design environments, CI/CD-based hardware flows, and managed open-source toolchains. Since 2018 he has been closely involved in the open-source silicon ecosystem, including the broader adoption of open PDKs such as SkyWater SKY130, which helped make practical open-source chip design possible. Under his leadership, Symbiotic EDA has supported customers and partners across industry, academia, and research, including IHP, Qualcomm, Huawei, and open-source chip-design initiatives connected to Google.

# Prof. Michael Athanassios Karagounis: Radiation-Hard Power Management and Control Circuits for the ATLAS Pixel Detector High-Luminosity Upgrade

**Abstract:** The High-Luminosity upgrade of the Large Hadron Collider (HL-LHC) will significantly increase the particle collision rate and place unprecedented demands on the detector electronics of the ATLAS experiment. The upgraded Inner Tracker (ITk) pixel detector must operate reliably in an extremely harsh environment characterized by high radiation levels, limited material budget, and a strong magnetic field of up to 4 T. The latter poses a particular challenge for power distribution, as conventional magnetic DC/DC converter technologies become impractical or impossible to deploy within the detector volume. This presentation provides an overview of the ATLAS pixel detector and its powering and control architecture. Particular emphasis is placed on radiation-hard power management integrated circuits developed to address the unique constraints of the HL-LHC environment. The design, implementation, and characterization of Shunt-LDO regulators for the detector's serial powering scheme will be discussed. These circuits enable efficient and reliable operation of large detector systems while minimizing power losses and material overhead. As an alternative powering approach, recent developments in high-frequency radiation-hard DC/DC converters will be presented. By operating at frequencies that allow the use of extremely small air-core inductors, these converters offer a promising solution for efficient local power conversion in the presence of strong magnetic fields. Their architecture, performance, and applicability to future detector systems will be discussed and compared with serial powering solutions. Beyond power delivery, reliable detector operation requires continuous monitoring and calibration of front-end electronics. The talk will therefore cover integrated monitoring concepts for pixel readout chips, including a radiation-tolerant automatic oscillator trimming technique that compensates for process, voltage, temperature, and radiation-induced variations without external intervention. Finally, the presentation will provide an outlook on future detector control architectures based on radiation-hard RISC-V microcontrollers. Ongoing developments toward fault-tolerant embedded control and monitoring platforms will be presented, highlighting their potential role in next-generation detector control systems for high-energy physics experiments. The presented work demonstrates how advanced radiation-hard mixed-signal and digital integrated circuits can address the unique challenges of the HL-LHC environment and enable robust powering, monitoring, and control of future particle detectors.

# Prof. Michael Athanassios Karagounis: Radiation-Hard Power Management and Control Circuits for the ATLAS Pixel Detector High-Luminosity Upgrade

**Bio:** Michael Athanassios Karagounis is Professor of Electronics at Dortmund University of Applied Sciences and Arts, Germany, where he leads research in integrated circuit design, radiation-hardened electronics, embedded systems, FPGA architectures, and AI hardware acceleration. He received a Dipl.-Ing. (FH) degree in Communications Engineering (Nachrichtentechnik) from the Technische Hochschule Köln and a Dipl.-Ing. degree in Electrical Engineering from the FernUniversität in Hagen. Prior to joining academia, he worked in the semiconductor industry as an Analog/Mixed-Signal Design Engineer at Infineon Technologies in Duisburg and as an RF Design Engineer at Intel Mobile Communications, also in Duisburg. His current research focuses on radiation-hard integrated circuits, power management systems for high-energy physics experiments, RISC-V-based embedded systems, FPGA and eFPGA architectures, and energy-efficient AI hardware accelerators. He is actively involved in the ATLAS experiment at CERN, where his group develops radiation-tolerant integrated circuits for detector powering, monitoring, and control in the challenging environment of the High-Luminosity Large Hadron Collider (HL-LHC). Prof. Karagounis leads several national and international research projects and collaborates closely with academic institutions, research laboratories, and industry partners. He is also co-leading the Intelligent Hardware Lab within the DFG Cluster of Excellence Color Meets Flavor, where he contributes to the development of next-generation intelligent detector electronics.

# Dr. Mahdi Taheri: Reliability vs. Security: Friends or Foes?

**Abstract:** Recent advances in Deep Neural Networks (DNNs) have significantly improved their accuracy, accelerating their deployment across diverse industrial and edge AI applications. However, these accuracy improvements are often achieved through increasingly complex models with millions of parameters, creating significant challenges for deployment in resource-constrained environments where power, area, and energy efficiency are critical concerns. Among such applications, safety-critical systems impose additional requirements on resilience, including both reliability and security guarantees. While resilience enhancement is essential to ensure trustworthy operation, its evaluation and mitigation often introduce considerable overheads, further complicating edge deployment. Moreover, many real-world systems require simultaneous assurance of reliability and security, as failures in either domain may ultimately lead to catastrophic consequences. This talk explores the interplay between hardware efficiency, reliability and security in edge AI systems, highlighting both their synergies and potential conflicts. The presentation will cover state-of-the-art resilience assessment methodologies, discuss the cross-dependencies between reliability and security vulnerabilities, and examine hardware-aware lightweight mitigation techniques designed for resource-constrained edge platforms

**Bio:** Mahdi Taheri received his Ph.D. from Tallinn University of Technology (TalTech), Estonia, in January 2025. He is currently a researcher at Brandenburg University of Technology (BTU) Cottbus-Senftenberg, Germany, and a part-time researcher at TalTech. He leads the Reliable and Secure Systems (RSS) team, focusing on reliable and secure AI systems, fault-tolerant design, neural network accelerators, approximate computing, and FPGA-based edge AI platforms.

## Mr. George Konstadinidis: Closing the gap between Reliability Physics, EDA and Circuit Design

**Abstract:** Accurate Circuit Reliability analysis is essential in reducing design margins, power, and time to market, while at the same time achieving high levels of product performance and reliability. The goal of this talk is to bring awareness and mutual understanding of the constraints across the various disciplines, and help strike a balance in the definition of the reliability rules, their implementation in EDA tools and their proper usage by the circuit designers. Following a brief description of the circuit reliability issues and the Physics behind them will describe some of the circuit techniques used to account for and mitigate these issues, and elaborate on the requirements imposed on the EDA tools. We will highlight common in situ monitoring and adaptive techniques to control the reliability and maximize performance over the lifetime of the product, and provide a brief introduction to final product reliability testing rules and test pattern requirements. Understanding how all this fits together is critical in establishing the skeleton of a Reliability Physics, EDA, and circuit design closed loop methodology.

## Mr. George Konstadinidis: The path from an R&D idea to a product

**Abstract:** What is the procedure and the University infrastructure requirements to materialize an R&D idea to a product? What should be the relationship between the University and the Industry? Financial and legal hurdles and requirements. IP protection and commercialization Funding stages and path to a successful and socially responsible business development.

**Bio:** Georgios Konstadinidis is a technology and HPC/AI HW Design consultant with 30+ years of experience. As a principal HW engineer at Google and prior to that as a senior HW architect at Sun Microsystems /Oracle, Georgios was involved in the technology strategy, physical design and custom circuit methodology, IC and systems reliability, CAD, power management architecture, IP evaluation, silicon bring-up and productization of numerous HPC CPUs and ML (TPU) systems. At the early stages of his career at SGS Thomson, Georgios was the RF design team lead involved in technology development and design of Telecommunication ICs, Georgios served at the ISSCC, IEDM, and IRPS Technical program committees, IRPS management committee and as Guest Editor at JSCC. Georgios has numerous IEEE publications and patents in the field of HPC design and is co-author of the “Clocking in Modern VLSI Systems” book. Georgios received his B.Sc. degree in Physics and the M.Sc. degree in Electronics and Telecommunications from the Aristoteles University Thessaloniki Greece, and his Ph.D degree in Electrical Engineering from the Institute of Microelectronics at the Technical University of Berlin, Germany.

# Prof. Yiorgos Tsiatouhas: Reliability Challenges in Computing-in-Memory Systems

**Abstract:** Computing-in-memory (CIM) electronic systems have emerged as a promising paradigm for overcoming the performance and energy limitations of conventional von Neumann architectures by integrating data storage and computation within a memory. This approach significantly reduces data movement, enabling high-throughput and energy-efficient execution of data-intensive applications such as artificial intelligence, machine learning, big-data processing, signal processing, and edge computing. However, CIM systems face substantial reliability challenges arising from the unique characteristics of emerging memory technologies and analog or mixed-signal computing operations. This lecture will provide an overview of the key reliability issues affecting computing-in-memory architectures. Topics will include process variations, manufacturing defects, device aging, radiation influence, retention failures, endurance limitations, read/write disturbances, and stochastic switching behavior like in emerging non-volatile memory technologies such as resistive RAM memory (RRAM) or phase-change memory (PCM). The impact of these phenomena on computational accuracy, inference performance, and long-term system robustness will be examined. The lecture will also discuss reliability challenges associated with analog and mixed-signal CIM operations, including testing and design for testability issues, noise, parasitic effects, thermal fluctuations, and variability-induced computational errors. Methods for reliability assessment, fault modeling, and error characterization will be introduced, together with contemporary mitigation strategies. By presenting recent research efforts, the lecture aims to provide a comprehensive understanding of the reliability bottlenecks that currently limit the adoption of computing-in-memory technologies. Participants will gain insight into the interdisciplinary approaches required to design robust, accurate, and energy-efficient CIM systems capable of supporting next-generation computing workloads.

**Bio:** Yiorgos Tsiatouhas received the B.S. degree in physics, the M.S. degree in electronic automation, and the Ph.D. degree in computer science from the University of Athens, Greece, in 1990, 1993, and 1998, respectively. From 1992 to 1996, he was with the National Center of Scientific Research “Demokritos,” Athens, Greece. From 1998 to 2002, he was with Integrated Systems Development S.A. as the Cooperative Projects Director and Technical Manager of the Advanced Silicon Solutions Group. In 2002, he joined the Department of Computer Science and Engineering, University of Ioannina, Greece, where he is currently a Full Professor. He was a recipient of the Best Paper Awards of the 2002 International Symposium on Quality Electronic Design and the 2009 IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems. He was a Program Committee Member of many international conferences in the area of VLSI design and design for reliability. He is senior member of IEEE and member of the IEEE Test Technology Technical Committee, as well as member of EDAA

# Prof. Georgios Karakonstantis: Beyond Worst-Case Design for Energy-Conscious Dependable Architectures

**Abstract:** Conventional dependable architectures are commonly designed under worst-case assumptions, relying on significant hardware redundancy and conservative safety margins to mitigate faults. Although such approaches provide high levels of reliability, they often lead to excessive energy consumption, increased design complexity, and higher implementation costs. This talk explores the concept of Beyond Worst-Case Design (BWCD) as an alternative paradigm for developing energy-efficient dependable systems. By recognizing that worst-case conditions occur infrequently, BWCD enables the use of adaptive techniques that optimize typical-case operation, while maintaining acceptable levels of reliability and output quality. The talk will discuss key approaches, including approximate computing, voltage overscaling and graceful degradation mechanisms aiming to foster new perspectives on the development of dependable architectures that are adaptive, energy-conscious and sustainable.

**Bio:** Georgios Karakonstantis is an Associate Professor in the Electrical and Computer Engineering Dept of University of Thessaly. He received his Ph.D. and MSc degrees from the Electrical and Computer Engineering department of Purdue University, U.S.A. His research on energy efficient and dependable architectures appears in more than 120 journals and conferences, 1 patent and 4 book chapters. He received the 'best paper award' at the IEEE DATE conference on 2020, and three 'paper awards' by the HiPEAC Network of Excellence on 2016, 2020, 2021. His work was also nominated for the 'best paper award' in the IEEE/ACM MICRO conference on 2020 and in the IEEE DATE conference on 2016, and was awarded a Prize at the International Altera Innovate Design Contest

# Dr. Artur Jutman: DFT Reuse Across Silicon Lifetime

**Abstract:** As multicore CPU subsystems grow in complexity, ensuring reliable operation in the presence of defects, PVT-caused uncertainty, aging, and in-field faults has become a major challenge. While Design-for-Test (DFT) infrastructures are typically limited to production use, they offer significant untapped potential for in-field monitoring for self-health awareness, resilience and prognostics. This talk explores how IC-level DFT hardware - such as scan chains, monitors, checkers and other embedded instrumentation (particularly following the IEEE Std. 1687 / IJTAG) - can be reused for runtime health monitoring, fault localization, and adaptive recovery. The talk will introduce architectural concepts that integrate DFT-based observability into system-level health management, enabling real-time anomaly detection and targeted mitigation demonstrated on a satellite case study. Focusing on multicore systems, we discuss key challenges such as distributed monitoring and coordinated recovery, and show how existing test resources can enhance robustness with minimal overhead. The talk highlights a shift toward viewing DFT as a runtime asset for building self-aware, resilient computing systems.

**Bio:** Artur Jutman has received a PhD degree in computer engineering from TalTech, Estonia in 2004. He has coordinated several EU-funded research consortia, participated in organizing conferences and workshops across Europe as well as given several keynotes, invited talks and tutorials at conferences and symposia. Dr. Jutman co-authored a textbook as well as over 160 peer-reviewed research papers on topics embracing embedded instrumentation, DFT, system health management as well as IC and system test in a broad sense. He is a founder and Managing Director of Testonica Lab company as well as a member of the steering committees of European Test Symposium, Estonian Electronics Industries Association, and the Nordic Test Forum society.

# Prof. John Goodacre: Innovation Management in the Age of LLMs: Accelerating Complex System Design

**Abstract:** Large Language Models are reshaping how organisations conceive, plan and execute complex engineering projects. This talk examines the implications for innovation management through a concrete case study: the end-to-end development of a production-grade networking system by a domain expert with no prior implementation experience, working exclusively through an LLM coding agent. The case illustrates a fundamental shift in the human role — from author to architect — where strategic direction, standards knowledge and quality judgement remain firmly human, while the LLM handles implementation at scale. The talk challenges established assumptions about the skills, team size and timelines required to innovate in complex technical domains and draws broader lessons for how managers and organisations can rethink resource allocation, expertise boundaries and the pace of innovation when LLMs enter the development loop.


**Bio:** John is Professor of Computer Architectures at the Department of Computer Science, The University of Manchester in the UK having previously spent 17 years with Arm Ltd as the Director of Technology and Systems. He was also appointed by UK government's Research & Innovation agency as the Director of the Digital Security by Design, a £200M programme to enable industry and researchers to create a step change in approach to cybersecurity – by design.

## Prof. Milan Dinčić: Neural Network Quantization

**Abstract:** The remarkable success of deep neural networks has enabled significant advances in computer vision, natural language processing, speech recognition, and many other application domains. However, state-of-the-art neural networks often require substantial computational resources, memory capacity, and energy consumption, which limits their deployment on resource-constrained devices such as embedded systems, edge platforms, and Internet of Things (IoT) devices. Neural network quantization is a model compression technique that addresses these challenges by representing network parameters and activations with reduced numerical precision. By replacing conventional floating-point representations with lower-bit fixed-point or integer formats, quantization can significantly reduce memory requirements, accelerate inference, and decrease energy consumption while maintaining competitive performance. This lecture provides an overview of the fundamental principles of neural network quantization, including uniform and non-uniform quantization methods. Special emphasis will be placed on quantization techniques that exploit the statistical properties of neural network parameters, an approach actively developed and investigated by the research team at the University of Niš. These methods aim to achieve excellent compression efficiency and accuracy preservation by adapting quantization strategies to the underlying parameter distributions.

## Prof. Milan Dinčić: Proposal Preparation: Lessons Learned from the AIDA4Edge and PEMS-ML Projects

**Abstract:** Preparing competitive project proposals requires not only strong scientific ideas but also a clear understanding of funding priorities, evaluation criteria, and proposal-writing best practices. This lecture summarizes practical experiences gained during the preparation and implementation of two different types of European projects: AIDA4Edge, a Horizon Europe Twinning project, and PEMS-ML, an Erasmus+ project, complemented by insights and recommendations obtained through training delivered by the AIDA4Edge partners. The goal of the presentation is to familiarize participants with these two project types and to share practical advice that may help improve the quality of future project proposals.

**Bio:** Prof. Milan Dinčić is an Associate Professor at the Faculty of Electronic Engineering, University of Niš. He currently serves as the coordinator of the AIDA4Edge project and the local coordinator of the Erasmus+ project PEMS-ML. He holds two Ph.D. degrees in distinct disciplines—Telecommunications and Metrology. In 2007, Prof. Dinčić was recognized as the Best Graduate Student of the University of Niš. He has authored more than 80 scientific publications, including 35 papers published in SCI/SCIE-indexed journals. His research interests include quantization, coding and compression theory, as well as the acquisition, processing, and modeling of sensor data for artificial intelligence applications. His work focuses on developing efficient methods for data representation and analysis, enabling advanced AI systems to operate effectively on resource-constrained platforms.

# Dr. Karthik Krishnegowda: EU-Band: A D-Band Joint Communication and Sensing System in a Eurostars Project

**Abstract:** EU-Band is a Eurostars-3 project. Three partners build a radio system for the D-band (110–170 GHz). The system does data communication and radar sensing at the same time. The carrier is near 135–140 GHz. First, I will explain how we built the Eurostars proposal: the goals, the consortium, the work packages, and the partner roles. Then I will show the technical side. IHP designs the transceiver chip in silicon-germanium (SiGe) BiCMOS. TERASi builds the antenna array and the package. IAF builds the software-defined radio and the field-programmable gate array (FPGA) backend. The system uses one shared waveform, OFDM (orthogonal frequency-division multiplexing), for both data and sensing. I will show our latest simulation results at 140 GHz. The radar detects a walking person with 0.969 probability. The range error is 2.2 cm. The data links stay error-free with channel coding. I will close with the test plan and how the partners plan to use the results.

**Bio:** Karthik Krishnegowda is a System Architect and Technical Project Manager at IHP – Frankfurt (Oder), Germany. He holds a Dr.-Ing. in electrical engineering from BTU Cottbus-Senftenberg (2020) and leads the system architecture for D-band integrated sensing and communication (ISAC) in the Eurostars-3 EU-Band project.

# Mr. Charalampos Samantzis: European Project Design and Management: Challenges and Opportunities

**Abstract:** Through the Centre for European Projects (CEP), the University of Thessaly (UTH) actively participates in a diverse portfolio of European research, innovation, and education initiatives. Leveraging its expertise in the design, development, and implementation of EU-funded projects, CEP supports researchers, academic staff, and administrative personnel in maximizing the impact and success of their activities within the European funding landscape.
The Centre for European Projects provides technical, administrative, and methodological support throughout the entire project lifecycle, from identifying funding opportunities and preparing competitive proposals to project implementation, management, and dissemination. It also offers expert guidance on major European funding programmes, organizes training and capacity-building activities, and facilitates collaboration through European networks and strategic partnerships, fostering excellence in research and innovation.


**Bio:** Mr. Charalampos Samantzis serves as Managing Director of the Center of International Education at the University of Thessaly, leading the University's internationalization strategy and coordinating competitive proposals under Erasmus+, Horizon Europe, CERV, ESF+, and other European programmes. He is a senior European project management and international cooperation expert with over 20 years of experience in the development, management, evaluation, and monitoring of EU-funded projects.
He is an authorized European Commission Expert Evaluator, Rapporteur, and Project Monitor, with extensive experience supporting major EU funding programmes. Throughout his career, he has contributed to more than 100 European projects across higher education, vocational education and training, digital transformation, sustainability, innovation, entrepreneurship, and regional development. He is widely recognized for his expertise in building international partnerships, developing high-impact proposals, and strengthening institutional capacity within higher education and research ecosystems.

# Dr. Marko Anđelković: An Overview of On-Chip Particle Detectors for Self-Adaptive Integrated Circuits for Space

**Abstract:** Integrated circuits employed in space missions are exposed to intense bursts of high-energy particles, such as heavy ions, protons and neutrons. If a single particle hits a sensitive transistor in an integrated circuit, data corruption or system failure may occur. With technology scaling it has become possible that a single particle hits multiple transistors, causing multiple errors. Thus, it is important to design electronic systems for space in such a way to ensure their sufficient robustness to radiation-induced effects.
As the particle flux in space can vary over several orders of magnitude, the most efficient approach is to use the adaptive protection mechanisms, which are activated only in the case of increased radiation intensity. To achieve this, dedicated particle detectors are required for continuous monitoring of radiation intensity. A cost-effective solution involves integrating particle detectors on the same chip with the target design.
In this talk, an overview of different solutions for on-chip detection of high-energy particle strikes in space missions will be presented. Special attention will be given to the particle detection solutions investigated and developed at IHP. The talk will compare the analyzed detectors in terms of their performance and requirements for readout electronics, emphasizing the key advantages and limitation of each detector. In addition, the design concept of a self-adaptive multi-core processing system for space applications will be presented.

**Bio:** Marko Anđelković received his Dipl-Ing. degree in Electronics from the Faculty of Electronic Engineering (University of Niš) in 2008. Since 2010 he was employed as a scientific researcher at the Faculty of Electronic Engineering in Niš, where he was working on characterization of custom-made dosimeters, evaluation of dosimetric properties of commercial semiconductor components, and design of readout electronics for experimental evaluation of various types of dosimeters. Since 2016 he is with IHP, where he is employed as a research associate within the System Architectures Department. His research interests include characterization and modeling of radiation-induced effects in digital circuits and rad-hard design. He has participated in numerous national, bilateral and EU-funded projects, and has authored/co-authored over 80 journal and conference papers.

# Prof. Davide Bertozzi: Cross-Layer Analysis of Permanent Faults in Asynchronous NoCs for Neuromorphic Computing

**Abstract:** Neuromorphic computing promises highly energy-efficient artificial intelligence through event-driven computation inspired by biological neural systems. A key enabler of this paradigm is the use of asynchronous communication, which more closely matches the clockless operation of the brain. Despite its importance, the reliability of asynchronous spike-routing hardware has received little attention. This talk presents the first cross-layer analysis of low-level hardware faults in an asynchronous neuromorphic Network-on-Chip (NoC), combining gate-level fault injection with spiking neural network simulation. The results show that localized routing faults can disrupt spike propagation through packet losses, misrouting, and packet insertion, with substantial consequences for inference accuracy. Remarkably, a single localized stuck-at fault can degrade application accuracy by up to 40%, revealing a level of vulnerability that is unique to neuromorphic communication fabrics. These findings establish communication reliability as a critical challenge for future neuromorphic systems and provide the foundation for fault-aware architectures and abstract behavioral models of routing errors.

**Bio:** Davide Bertozzi is a Reader in Advanced Processing Technologies at University of Manchester (United Kingdom). He got his PhD at University of Bologna (Italy) in 2003 and led the multiprocessor system-on-chip group at University of Ferrara till 2023. The mission of his research is to stay at the forefront of system innovation by leveraging the enabling properties of interconnection architectures and emerging technologies. He has been visiting researcher at Stanford University and at several semiconductor industries (STMicroelectronics, NEC America Labs, NXP, Samsung). In 2018 he received the Wolfgang Mehr Award from IHP Microelectronics, a Leibniz Institute for innovative microelectronics in Germany, for his interdisciplinary research on photonically-integrated systems. His research interests span widely across the field of on-chip communication with a strong drive to overcome the communication bottleneck in emerging system architectures, ranging from neuromorphic computing to multi-tenant fog nodes. He currently contributes to the activities for neuroscience simulation acceleration within the flagship EBRAINS 2.0 project, and takes part to a collaborative effort to bring the celebrated SpiNNaker large-scale neuromorphic computing platform to the next generations of technology, implementation and architecture. Finally, he is deeply involved in recent EU-funded initiatives (TAICHIP, TWIN-RELEC, AIDA4Edge) to enhance networking between research institutions of the widening countries and top-class leading counterparts, encompassing joint research, knowledge transfer and exchange of best practices in the fields of AI chips, open EDA tools and hybrid SNN-ANN models, respectively. His scientific activity has led to roughly 200 publications, with five best paper awards, three best paper award nominations and one high-impact paper award for one of the five most cited papers in the first thirty years of the Int. Conference of Computer Design.

# Dr. Fabian Luis Vargas: Combined Effects of Ionizing and Non-Ionizing Radiation: From Simulation to Practical Experiments

**Abstract:** Technology scaling, which made electronics accessible and affordable for almost everyone on the globe, has advanced IC and electronics since sixties. Nevertheless, it is well recognized that such scaling has introduced new (and major) reliability challenges to the semiconductor industry. This tutorial addresses the background mechanisms impacting reliability of very deep submicron (VDSM) integrated circuits (ICs). Topics such as the basics about EMC and ionizing radiation, the mechanisms by which they affect ICs, the current standards and laboratory test setup for electromagnetic compatibility (EMC), total-ionizing dose (TID) and single-event effects (SEEs) on ICs are presented and their combined effects on the reliability of modern ICs are discussed. Reliability failure mechanisms for (ionizing and non-ionizing) radiation, the way they are modeled and how they are impacting IC lifetime will be covered. Laboratory test setup and recent results from experimental measurements are described. Classic design solutions to counteract with TID, SEEs and EMI in VDSM ICs as well as the recent achievements on the development of on-chip sensors to monitor EM conducted noise on IC power supply lines of ICs are introduced. Spice simulations are used to demonstrate the combined effect of ionizing radiation with power supply noise on SRAM cells followed by the presentation of some measures to counteract with it.

**Bio:** Fabian Vargas obtained the Ph.D. Degree in Microelectronics from the Institut National Polytechnique de Grenoble (INPG), France, in 1995. At present, he is Senior Scientist at IHP – Leibniz Institute for High Performance Microelectronics, Germany, where he works on the design of on-chip sensors and cross-layer resilience for aerospace systems. Vargas has served as Technical Committee Member and Guest-Editor in many IEEE-sponsored conferences and journals. He holds several patents and published over 200 refereed papers. Vargas was researcher of the BR National Science Foundation from 1996 to 2023. He co-founded the IEEE-Computer Society Latin American Test Technology Technical Council (IEEE LA-TTTC) in 1997 and the IEEE Latin American Test Symposium (LATS) in 2000. He received the Meritorious Service Award of the IEEE Computer Society for providing significant services as chair of these groups. Vargas is Golden Core Member of the IEEE Computer Society and Senior Member of the IEEE.

# Prof. Luigi Dilillo: Error Monitoring and Hardening on the HARV (RISC-V) Microcontroller

**Abstract:** Fault tolerance in processors designed for harsh radiation environments is traditionally achieved by implementing microarchitectures with spatial, temporal, or information redundancy at different abstraction levels. Techniques such as Triple Modular Redundancy (TMR) and Error-Correcting Codes (ECC) with SECDED are commonly used to automatically detect and correct Single-Event Effects (SEEs). However, these mitigation methods usually mask errors in the background, which restricts the application's visibility regarding the actual error rates and the error propagation of radiation-induced faults. With the growing adoption of the open-standard RISC-V Instruction Set Architecture (ISA) as a customizable and scalable baseline for modern space and avionic applications, ensuring structural dependability is critical. To provide an exhaustive analysis of errors within such systems, this presentation introduces microarchitectural and system-level observability mechanisms developed for a fault-tolerant RISC-V implementation, specifically the HARV (Hardened RISC-V) processor and its System-on-Chip (HARV-SoC). The proposed design incorporates a dedicated hardware error handler into the processor core, working in parallel with an exclusive SoC error handler at the bus controller level. When a single- or double-bit upset is detected in the core or external SDRAM memory, the error handlers temporarily store the fault metadata alongside a rotating queue that captures the application's execution context. Instead of silent correction, these events are reported directly to the application layer via exceptions, synchronously interrupting the application flow to allow immediate logging and analysis. This fault awareness approach has been thoroughly characterized and validated through a series of experimental testing campaigns at accelerated particle accelerator facilities, including atmospheric neutron testing at ChipIr, high-energy proton testing at PARTREC and PSI, and mixed-field testing at CHARM. The telemetry provided by the exception-driven reports enabled the identification and classification of rare, complex events, such as uncorrectable Single-Event Functional Interrupts (SEFIs) and multi-address memory block errors in the external SDRAM. This fault tracking infrastructure provides the necessary visibility into the system's operational health, enabling the development of targeted software recovery routines, such as checkpoints and rollbacks, to enhance the overall dependability of embedded RISC-V platforms in space and avionic applications.

**Bio:** Luigi Dilillo received his master's degree in Electronic Engineering from the Politecnico di Torino, Italy, in 2001, with specialization in Microelectronics. He received his Ph.D. degree in Information, Structures, and Systems from the University of Montpellier, France, in 2005. He did a post-doc at the University of Southampton, United Kingdom, from 2005 to 2007. He is currently a researcher and leader of RADIAC team at IES (University of Montpellier).

# IEEE SB UTH: Meet the IEEE Student Branch & WIE Affinity Group of Volos

**Abstract:** The IEEE Volos Student Branch is a local chapter of the world's largest technological professional organization that fosters skill development through workshops, competitions, and hands-on activities. Led by a five-member executive team, the branch actively engages in diverse technical initiatives ranging from ethical hacking to aerospace engineering.
IEEE Women in Engineering Student Branch University of Thessaly, Volos is a student-led community dedicated to empowering, supporting, and inspiring future engineers and scientists. Through educational activities, talks, workshops, seminars, and creative STEM events, WIE Volos promotes an inclusive environment where students can develop their technical, professional, and soft skills.
Our goal is to encourage more young people, especially women, to explore STEM, build confidence, share ideas, and pursue their academic and career ambitions. By highlighting the achievements of women in engineering, science, technology, and innovation, WIE Volos strengthens diversity, collaboration, creativity, and leadership within the University of Thessaly and the wider local community.

**Bio:** Mr. Panagiotis Balamotis is a 4th-year ECE undergraduate at the University of Thessaly, passionate about cybersecurity and programming. He currently serves as the Secretary for IEEE SB Volos and Co-Manager of the university's ethical hacking team, Broken Shells.

**Bio:** Eleftheria Litou is a final-year ECE student with interests in EDA, ASIC, and FPGA design. Experienced in VLSI design, CAD implementations, TCAD Simulations, and full ASIC flow. Also interested in Web Development. Beyond the lab, she has dedicated the last 6 years to the IEEE SB in Volos. Currently serving as the Head of the IEEE WIE SB in Volos. Also she spent over four years as the PR Manager for both IEEE and WIE. Additionally, she has contributed as a volunteer to numerous conferences and actively support the academic process as a volunteer teaching assistant for university courses.

**Bio:** Evangelos Toris is a 4th-year undergraduate student in Electrical & Computer Engineering and a Taekwondo athlete at the University of Thessaly and Nikomahos Club. He is interested in Technology, Electronics, Business Management and Sports. Since 2025, he is dedicated to advancing the Student Technological Society, serving as Treasurer of the IEEE SB Thessaly - Volos.