



2nd TWIN-RELECT Training School



“Design of Reliable Integrated Circuits”

Technical Program

**IHP - Leibniz Institute for High Performance Microelectronics
Frankfurt (Oder), Germany**

19 - 20 May 2025

Monday, 19th May

9:00 – 9:45: Registration

9:45 – 10:00: Opening Session and IHP's Welcoming Address

Fabian Vargas, Marko Andjelkovic, Milos Krstic

10:00 – 10:15: TWIN-RELECT: Twinning for Excellence in Reliable Electronics

Christos Sotiriou, University of Thessaly, Volos, Greece

10:15 – 11:15: Keynote Talk 1

Cell-Aware Testing for Robust Circuit Design

Rene Krenz-Baath, TH Wildau, Wildau, Germany

11:15 – 11:45: Coffee-Break

11:45 – 13:15:

Session 1 - Radiation-Hardened Integrated Circuits for Space

11:45 – 12:30: Lecture 1: ASICs for Space: Design Examples

Filip Ostrovskyy, IHP, Frankfurt (Oder), Germany

12:30 – 13:15: Lecture 2: Peakrad – Radiation-Hardened Microcontroller for Space

Felipe Kuentzer, IHP, Frankfurt (Oder), Germany

13:15 – 13:15: Lunch

13:15 – 14:45:

Session 2 - Reliability of Emerging Technologies

13:15 – 14:00: Lecture 3: Heterogeneous Integration in AI Computing: Challenges and Solutions

Leticia Bolzani Poehls, IHP, Frankfurt (Oder), Germany

14:00 – 14:45: Lecture 4: HfO₂-Based RRAM Technology as a Candidate for In-Memory Computing in Harsh Radiation and Ultra-Low-Temperature Environments

Emilio Perez Bosch Quesada, IHP, Frankfurt (Oder), Germany

14:45 – 15:45:

PhD Forum (Short presentations – 8 min.)

Talk 1:

Georgos-Ioannis Paliaroutis, University of Thessaly, Greece

Fault Injection Attacks Based on Layout-Driven SER Analysis

Talk 2:

Nikos Chatzivangelis, University of Thessaly, Greece

Reliability Analysis of Clock Networks Using Custom Simulation Tools

Talk3:

Nikolaos Zazatis, University of Thessaly, Greece

Reliability Analysis on Dynamic Neural Network

Talk 4:

Pelopidas Tsoumanis, University of Thessaly, Greece

SET Models for Generation and Propagation

Talk 5:

Dimitrios Tsalapatas, University of Thessaly, Greece

Post-Placement Timing Optimizations on Asynchronous Designs

Talk 6:

Christos Georgakidis, University of Thessaly, Greece

Closed-loop, Fully-automated Flows for SET Mitigation

Talk 7:

Nicola Miglioranza, IHP, Germany

Radiation Hardened Baseband Processor for Satellites

[15:45 – 16:15: Coffee-Break](#)

16:15 – 17:15:

PhD Forum (Posters)

17:15 – 18:15:

TWIN-RELECT Meeting

Discussion on current status of joint research activities

Tuesday, 20th May

09:15 – 10:15:

Visits to IHP Clean Room and Test Laboratory

10:15 – 11:15: **Keynote Talk 2**

Low-Cost and Fault-Tolerant Routing in Networks on Chip

Daive Bertozzi, University of Manchester, UK

11:15 – 11:45: Coffee-Break

11:45 – 13:15:

Session 3 - Fault-Tolerance Analysis Methodologies (Part 1)

11:45 – 12:30: Lecture 5: Using Machine Learning for Simulation-Based Fault Injection

Li Lu, IHP, Frankfurt (Oder), Germany

12:30 – 13:15: Lecture 6: Fault Analysis Techniques for Dependable AI

Alessandro Veronesi, IHP, Frankfurt (Oder), Germany

13:15 – 14:15: Lunch

14:15 – 15:45:

Session 4 - Fault Tolerance Analysis Methodologies (Part 2)

14:15 – 15:00: Lecture 7: Laser Illumination as a Means of Data Modification in Semiconductor Devices

Dmytro Petryk, IHP, Frankfurt (Oder), Germany

15:00 – 15:45: Demo: Introduction to UPSET Tool

Christos Georgakidis, University of Thessaly, Volos, Greece

15:45 – 16:00: Closing Session

Fabian Vargas, Marko Andjelkovic, Milos Krstic

19:00 – 22:00:

Social Event – Dinner at Restaurant “Villa Casino”, Slubice, Poland

<https://villa-casino.pl/de/>

(Non-EU citizens should take passports due to possible border control)

Notes:

1. *Certificates will be provided to the participants of the 2nd Training School at the end of the event.*
2. *All participants will have opportunity to express their opinion about the event by completing an Evaluation Form on the last day.*
3. *All sessions will take place in room D1 (first floor)*

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